is extremely useful, since arsenic has a relatively low diffusivity. The use of a refractory material for the gate electrode minimizes the space required for the upper electrode system of the device, since the metal source electrode can overlie the refractory gate electrode. Additionally, by forming the gate oxide late in the process of manufacture, with minimal thermal cycling, the gate becomes relatively insensitive to radiation damage. The device, in fact, exhibits a relatively flat curve of threshold gate-to-source voltage as a function of total radiation dose up to and exceeding 1 megarad.

Although the present invention has been described in connection with a plurality of preferred embodiments thereof, many other variations and modifications will now become apparent to those skilled in the art. A non-cellular vertical conduction device can be formed rather than the multicellular device described above, for example. Also, the invention is not limited to vertical conduction devices, and applies to lateral conduction devices. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A process of manufacturing a depletion mode power MOSFET with a refractory gate electrode, comprising the steps of:

forming a base region of one conductivity type in a layer of semiconductor material of the opposite conductivity type by process steps including introducing dopant of the one conductivity type into an upper surface of said layer at a selected location and thermally driving said dopant to a first depth beneath the surface by maintaining said layer at a high temperature;

forming a source region of the opposite conductivity type in said base region by process steps including introducing and driving dopant of the one conductivity type into the upper surface of said layer at a selected location to a second depth which is less than said first depth, with the periphery of said source region being spaced from the periphery said base region at said surface;

forming a depletion channel region at the upper surface of said previously formed base region by introducing dopant of the one conductivity type into said base region; and

thereafter forming a gate oxide over said depletion channel region, a refractory gate electrode over said gate oxide, a dielectric layer over said gate electrode and a source electrode contacting said source region by process steps employing temperatures lower than said high temperature used to form said base region.

2. The process of claim **1**, wherein said high temperature is greater than about 1050° C. and wherein said process temperatures following the formation of said depletion channel region are less than about 950° C.

3. The process of claim **1**, wherein the dopant employed for forming said depletion channel region has a diffusivity less than that of phosphorous.

4. The process of claim **3**, wherein said dopant for forming said depletion channel region is arsenic.

5. The process of claim **1**, wherein said base source and channel depletion region define a cell, and further comprising the steps of simultaneously forming a plurality of further cells in the same manner as said first-mentioned cell, so as to form a multicellular device.

6. The process of claim **1**, wherein said depletion channel region is less than about 5000 angstroms deep.

7. The process of claim **1**, wherein said refractory gate electrode comprises polysilicon.

8. The process of claim **1**, wherein said refractory gate electrode comprises a refractory metal.

9. The process of claim **1**, wherein said refractory gate electrode comprises a a refractory silicide.

10. The process of claim **1**, wherein said gate oxide is formed by a pyrogenic process.

11. The process of claim **1**, which further includes the step of annealing said gate oxide after the formation thereof.

* * * * *